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A. Asthana , H. V. Jagadish , J. A. Chandross , D. Lin , S. C. Knauer
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Bart Kienhuis , Ed Deprettere , Kees Vissers , Pieter van der Wolf
Proceedings of the 6th international workshop on Hardware/software codesign March 1998

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Jeffrey Dean , James E. Hicks , Carl A. Waldspurger , William E. Weihl , George Chrysos
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Profile data is valuable for identifying performance bottlenecks and guiding optimizations. Periodic sampling of a processor's performance monitoring hardware is an effective, unobtrusive way to obtain detailed profiles. Unfortunately, existing hardware simply counts events, such as cache misses and branch mispredictions, and cannot accurately attribute these events to instructions, especially on out-of-order machines. We propose an alternative approach, called ProfileMe, that samples instructio ...

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Proceedings of the seventh international conference on Architectural support for programming languages and operating systems September 1996
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Designer's productivity has become the key-factor of the development of electronic systems. An increasing application of design data reuse is widely recognized as a promising technique to master future design complexities. Since the intellectual property of a design is more and more kept in software-like hardware description languages (HDL), successful reuse depends on the availability of suitable HDL reverse engineering tools. This paper introduces new concepts for an integrated HDL reverse eng ...

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set simulator, 40,000 for a clock-**cycle accurate simulator** and 500 for an **RTL** accurate simulator
for a clock-**cycle accurate simulator** and 500 for an **RTL** accurate simulator in VHDL. Simulating, for
as C functions within the PAMELA run-time library (**RTL**)This is a multithreading package that performs
ptolemy.eecs.berkeley.edu/~kienhuis/ftp/codes98.pdf

A High-Level Hardware Design Methodology using C++ - Roth, Ramanathan (1999) (Correct)
Furthermore, our class library provides a **cycle-accurate simulator** that enables creation of cycle wrapped
designs from a purely functional level to low level **RTL** while remaining in a single unified design
as Verilog and VHDL were initially centered around **RTL** designs. Higher levels of abstraction were more
www.ics.uci.edu/~dinesh/pubs/hldvt99.ps.Z

A Method to Construct Reconfigurable Simulators from.. - Bart Kienhuis (1997) (Correct)
the SPIM simulator in table I, the clock-**cycle accurate simulator** tmsim is given. Going down level in
CClock-Cycle 10.000 3.6 Hrs (dataflow) Dlx Vhdl **Rtl** 500 30 Days (dlx) A Processor Simulator (e.g.
paper. If we go down one more level in accuracy, the **RTL** level simulator DLX is given that has a factor 200
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bandwidth in the interconnection between the **processors** and the memories, coupled with long delays
by using static analysis to estimate the **performance** improvement afforded by our prefetching
realistic shared-memory system using an **RTL**-level **simulator** and real codes. This differs from previous
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produces optimized machine code for target **processors** with different instruction set architectures.
thus allows us to accurately evaluate the **performance** of different architectures on application
system is evaluated using a hardware-software co-**simulator**. The partitioning and **processor** design are
glen.lcs.mit.edu/~devadas/pubs/aviv.ps

Automatic Generation of Microarchitecture Simulators - Önder, Gupta (1998) (Correct) (2 citations)
three **simulators** ranging from simple pipelined **processors** to complicated out-of-order issue **processors**
studies are carried out to estimate the expected **performance** of the microarchitecture on a variety of
Automatic Generation of Microarchitecture **Simulators** Soner Onder Rajiv Gupta Department of
www.cs.pitt.edu/~soner/publications/iccl98.ps

Application-driven Design Automation for Microprocessor Design - Iksoo Pyo (1992) (Correct) (2 citations)
design space and synthesize a single chip VLSI **processor** from a high-level specification of the
used to motivate design decisions and optimize **performance**. Compiler optimizations are considered during
consists of a Semantic Design Generator (SDG)a **simulator**, an evaluator, a translator, a design library,
www.isi.edu/acal/tech-reports/1992/tr-92-03.ps.Z

A Design Experience of A GaAs Datapath Generation Using.. - Moussa, GUYOT (Correct)
like microprocessors or Digital Signal **Processor** (DSP) circuits. In this way the designer can
onto a GaAs technology library to achieve high **performance** regarding speed, area and power consumption.
Transistor level Timing verification HSPICE **Simulator** Place and route return to the source file No!
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of the latency and throughput of the inter-**processor** interconnection network. In the experiments we
{livio, lincoln, meseguer}csl.sri.com Keywords: **Performance** evaluation, Distributed simulation of computer
distributed event causality relations. The **simulator** correctly executes a given parallel application
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Synthesis of TTL Specification: A Case Study - Carchiolo, Malgeri, Mangioni (Correct)
an architecture including a single generalpurpose **processor**, a few application-specific hardware components
Project "Design Methodologies and Tools of High **Performance** Systems for Distributed Applications" power
tested. The Formal Tools block also comprises a **simulator** which is used during specification and the
www.cdc.unict.it/~carchiol/articoli-mosaico/Cesa98.ps

EEL: Machine-Independent. . . - Larus, al. (1995) (Correct)
computer from the logical cycle times of **processors** directly executing a parallel program. The
fault isolation, architecture translation, **performance** measurement, simulation, and optimization
example, the Wisconsin Wind Tunnel architecture **simulator** [19] drives a distributed, discrete-event
ftp.cs.wisc.edu/wwt/pldi95_eel.ps

Inter-Domain Movement of Functionality as a Repartitioning.. - Stoy, Peng (1995) (Correct)
implementation is considered as a specialized co-**processor** which will be controlled by and interact with

new versions of a product to offer other cost/**performance** trade-offs. One obvious way to achieve (Re-Partitioning Transformation/ Optimization **Simulator** Fig. 2 Design environment. 3 -tasks such ftp.ida.liu.se/pub/labs/cadlab/reports/r-95-33.ps.gz

Evaluation of Design Error Models for Verification Testing.. - Van Campenhout, al. (Correct)
instruction set architecture (ISA) model of the **processor**. Both models are assumed to be executable. A is an essential activity in the design of high-**performance** microprocessors, especially for concluding remarks are given in Section 5. **RTL simulator** Specification **simulator** Equal? Diagnose & www.eecs.umich.edu/~tnm/papers/mtv98.ps

Towards a Unified Analysis Methodology of HW/SW Systems based.. - Castillo, al. (Correct)
which can be quite complex themselves (e.g.**processor** cores, microcontrollers, floating point and block consists of a HW-part and a SW-part, the **performance** of such a BB is determined by the HW debugging features are provided by the ASM **simulator**. In this paper, after a short overview of some ftp.eecs.umich.edu/groups/gasm/hwswmodel.ps.gz